UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,632	07/17/2003	Todd C. Adelmann	200208962-1	9968

22879 7590 12/06/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 12/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,632	ADELMANN ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The present Office Action is taken in response to applicant's communication filed.

2. Claims 1-22 are pending in the application under prosecution.

Response to Arguments

3. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,717,648 (Davis et al) in view of US 2002/0167829 (Friedman et al).

With respect to claim 1, 10, and 19, Davis teaches the invention as claimed, an integrated circuit device that comprises: a memory array integrated on a substrate, the memory array storing data in encoded form *[(storage area storing encoded equivalent of HITA-D lines encoded by encoders) Col. 12, Lines 45-49; Col. 15, Lines 1-2]*; a decoder integrated on said substance, coupled to the memory array and configured to decode

data retrieved from the memory *[(received index addresses to be decoded by master line decoder MWL0 DECODE) Col. 7, Lines 56-67]*; and a cache integrated on said substrate and coupled to the memory array *[cache integrated with the other circuitry on the microprocessor) Col. 6, Lines 6-11]*, wherein the cache is configured to retrieve data stored in the memory array in anticipation of a request for said data *[(cache typically made of arrays of SRAM cells to be accessed at rates faster than accesses of DRAM cells) Col. 1, Lines 23-32; Col. 6, Lines 12-21]*. Davis fails to specifically teach the cache and the memory array being separate entities that are coupled together. However, Friedman teaches an integrated circuit is provided comprising a substrate, a cache memory array in the substrate, and a three-dimensional primary memory array on the same substrate, Fig. 2 shows a three-dimensional cache system 400 comprising a solid-state three-dimensional memory array 410 coupled with control logic 420 and a cache memory 430 [abstract; Fig. 2; Paragraphs 0023, 0005]. Therefore it would have been obvious to one of ordinary skill in the art to have the cache and the memory array being separate entities coupled together on the same substrate, as taught by Friedman, because this would have eliminated inter chip transmission delays that would have been an issue in multi chip arrangements. Friedman additionally teaches the cache memory array being used to temporarily store (1) data that is later to be stored in the three-dimensional primary memory array and/or (2) data that was previously stored in the three-dimensional primary memory array [paragraphs 0019; 0024].

With respect to claims 2-9, 11-18, and 20-22, the combination of Davis and Friedman discloses:

the decoder coupled between the memory array and the cache and the cache storing decoded data (Davis: Fig. 4; Col. 12, Lines 45-49; Col. 7, Lines 56-67; Fig. 4).

the cache coupled between the memory array and the decoder and wherein the cache stores encoded data, the encoded data consisting of error detection codes, error correction codes and encryption codes (Davis: Fig. 4; Col. 12, Lines 45-49; Col. 7, Lines 56-67; Fig. 4)

a selection circuit coupled to the memory array to select a set of one or more memory cells in response to an address value; and a sense circuit coupled to the memory array to sense data stored in the selected set of memory cells, wherein the cache is configured to receive a read operation comprising an address value, and is further configured to provide the address value to the selection circuit if the cache does not have a copy of data stored in the corresponding set of memory cells [Davis: Fig. 3, 11B; Col. 10, Lines 44-46].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

November 27, 2006